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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,126	07/22/2003	Yil-suk Yang	2013P096	8801

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EXAMINER	
SUN, SCOTT C	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 11/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,126	YANG ET AL.	
	Examiner	Art Unit	
	Scott Sun	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/22/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 3 and 6 are objected to because of the following informalities: claim 3 recites a second three-phase "bus" where "buffer" is expected; claim 6 recites "an" in line 3 where "and" is expected. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 5-8, 10-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Regarding claim 5, 6, 10, 12, and 13, "third", "fourth" ... and "ninth" three-phase buffer implies there are other three-phase buffers previously mentioned. However, there is a lack of antecedent basis for these additional buffers in the parent claims. The examiner reminds the applicant that because the above cited claims do not all depend on each other, a relationship between them should not be implied. For example, claim 5 depends on claim 1, but not claim 3, therefore the two buffers mentioned in claim 3 are not necessarily present in the invention described by claim 5. Therefore, the "third" buffer mentioned in claim 5 should be referred to as a "first" buffer, as it is the first explicit disclosure of such limitation in claim 5 and its parent claims.

5. Regarding claims 7, 8, 11, and 14, they are rejected because of their dependence on the above rejected claims.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Little et al (PG Pub #US 2001/0011353).

8. Regarding claim 1, Little discloses a data bus system (figure 1) that has an input/output unit (UART - Universal Asynchronous Receiver Transmitter), a central processing unit (ALU), an internal memory (ROM, SRAM), and a peripheral circuitry (CRC, Math co-processor, Timed Access, note the examiner interprets peripheral circuits as any on-chip circuit that is not the CPU, memory, nor the I/O unit) the data bus system comprising: an external access bus used when data is output from the CPU or data is input to the I/O unit or the internal memory unit (control/data bus section below ALU; paragraph 38); an internal access bus used when data is input to the CPU, data is output from the I/O unit, or the internal memory unit, or data is input to or output from the peripheral circuitry (control/data bus section above ALU; paragraph 38); and an

internal memory test bus used when data is output from the internal memory unit and input to the I/O unit (control/data bus section connecting SRAM/ROM to UART). The examiner asserts that a statement with multiple elements separated by "or" is true if any of the elements is true. In the instant case, prior art anticipates the limitation "data is output from the CPU or data is input to the I/O unit or the internal memory unit" if at least one of "output from the CPU", "input to the I/O unit", or "input to the internal memory unit" is taught. The same argument is applied to the limitation "an internal access bus used when data is input to the CPU, data is output from the I/O unit, or the internal memory unit, or data is input to or output from the peripheral circuitry".

9. Regarding claim 9, Little discloses the data bus system of claim 1, further comprising: a data port used to transmit external data (figure 4, one-wire); a data port control block which controls data in the data port (control logic); an external data bus which acts as a path of the movement of data among the data port, the data port control block, and the external access bus (arrows connecting one-wire, control logic, and data/control bus).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Little et al (PG Pub #US 2001/0011353) in view of Alvarez (US Patent # 6,725,307).

12. Little discloses claim 1, but does not disclose explicitly a latch structure connecting buses. However, Alvarez discloses a latch structure connecting buses (figure 6, paragraph 33). The teachings of Alvarez and Little are from analogous art of processing systems.

Therefore, it would have been obvious at the time of invention to combine the teachings of Alvarez and Little by implementing a latch structure connecting to buses in the system disclosed by Little for the benefit of providing a fixed and predetermined delay (Alvarez, paragraph 34)

13. Claims 3, 5-8, 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Little et al (PG Pub #US 2001/0011353) in view of Klaas (US Patent # 6,816,750).

14. Regarding claims 3, 5, 6, 10, 12, and 13, Little discloses substantial features but does not disclose explicitly the use of tri-state buffers between buses and on-chip devices (CPU, memory, i/o unit, and peripherals). However, Klaas teaches the use of tri-state buffers in connecting on-chip devices to buses (column 4, lines 23-32). Little's invention and Klaas's invention are from the analogous art of microprocessors.

Therefore, it would have been obvious to a person of ordinary skill in the art to apply Klaas's teachings by placing tri-state buffers between each of the on-chip devices and the buses in the system disclosed by Little for the benefit of reducing logic and die area used to implement the microprocessor (Klaas, column 4, lines 47-51)

15. Further regarding claim 3, Little discloses a CPU read bus which acts as a path of the movement of data between the CPU and the internal access bus (figure 1, solid arrows entering ALU), and a CPU write bus which acts as a path of the movement of data between the CPU and the external access bus (solid arrow exiting ALU).

16. Further regarding claim 5, Little discloses a peripheral circuitry read bus that acts as a path of the movement of data from the peripheral circuitry to the internal access bus (figure 1, double arrows connecting peripheral circuitry to data/control bus, see list of peripheral circuitry pointed out by the examiner in paragraph 8); and a peripheral circuitry write bus which acts as a path of the movement of data from the internal access bus to the peripheral circuitry (figure 1, double arrows connecting peripheral circuitry to data/control bus, see list of peripheral circuitry pointed out by the examiner in paragraph 8)

17. Regarding claims 7, 11, and 14, although Little and Klaas combined does not disclose expressly using AND or OR gates. However, the examiner asserts that in data bus systems, it is well known in the art at the time of invention to control bus access from different devices using AND or OR gates. Therefore it would have been obvious to implement such gate logic in Little's invention. The motivation for doing so would have been to regulate bus access to prevent multiple and simultaneous writes, which produce erroneous results, to a single data bus.

18. Regarding claim 8, although Little and Klaas combined does not disclose expressly using a system clock. However, the examiner asserts that in microprocessors, it is well known in the art at the time of invention to implement a

system a clock to synchronize and control hardware devices. Without a system clock (a timer), hardware devices within a microprocessor would be unable to function at the time of invention. Therefore, it would have been obvious to implement such a clock to control memory access for the benefit of synchronizing operation of hardware devices.

19. Regarding claim 4, although Little and Klaas combined does not disclose explicitly memory read and write control blocks used to transfer data between the buses and internal memory, one of ordinary skill in the art would readily implement control mechanisms to transfer data in and out of memory, because without them the memory would be not function.

20. Other publications are cited to further show the state of the art with respect to bus systems and microprocessor design. Refer to form 892, "Notice of References Cited", for a complete list of relevant prior arts cited by the examiner.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Sun whose telephone number is (571) 272-2675. The examiner can normally be reached on M-F, 10:30am-7pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

11/10/05

KIM HUYNH
PRIMARY EXAMINER
11/18/05